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# Sanan Product Brochure SiC and GaN Material

N-type SiC Substrate

## Company Profile

Sanan Semiconductor Co., Ltd (Sanan Semiconductor), as a wholly-owned subsidiary of the listed company Sanan Optoelectronics (600703CH), is a manufacturer focusing on the power electronics field, providing power semiconductor materials and foundry services.

We are the technology commercialization leader with the capacity and scale to bring large diameter wafers and high-quality epitaxy to the market in mass production volumes.

Sanan Semiconductor has long-proven expertise in SiC and GaN materials technology advancement. We have achieved stable supply to over 20 domestic and international customers. Our current production capacity includes 360,000 6-inch wafers and 520,000 8-inch wafers annually, with a long-term planned capacity of 1 million wafers per year. Our products primarily serve the manufacturing of SiC MOSFETs, with end applications spanning automotive, photovoltaic and energy storage systems (PV & ESS), charging infrastructure, power supplies, and home appliances.

Polytype	Single-Crystal 4H	
Supported diameters	150 mm & 200 mm	
Crystal structure	Hexagonal	
Bandgap	3.26 eV	
Thermal conductivity (n-type; 0.020 Ω·cm)	a~4.2 W/cm · K @ 298 K	c~3.7 W/cm · K @ 298 K
Lattice parameters	a=3.073 Å	c=10.053 Å
Mohs hardness	9	

<b>n-TYPE SiC Substrate</b>	<b>High Purity Semi-insulating SiC Substrate</b>	<b>SiC Optical Substrate</b>
<b>SiC Heatsink Substrate</b>	<b>SiC EPITAXY</b> n-type and p-type Epitaxial Layers	<b>NITRIDE EPITAXY</b> GaN, AlGaIn, AlInN Epitaxial Layers

## DIMENSIONAL PROPERTIES, TERMINOLOGY AND METHODS\*

### DIMENSIONAL

The linear dimension across the surface of a wafer. Measurement is performed using an automated optical micrometer, providing the average value for each individual wafer.

### THICKNESS,CENTER POINT

Measured with non-contact tools at the center of each individual wafer.

### SURFACE ORIENTATION

Denotes the orientation of the surface of a wafer with respect to a crystallographic plane within the lattice structure. In wafers cut intentionally “off orientation,” the direction of cut is parallel to the primary flat or notch, away from the secondary flat (if present). Measured with x-ray goniometer on a sample of one wafer per boule in the center of the wafer.

### ORTHOGONAL MISORIENTATION

In wafers intentionally cut “off orientation,” the angle between the projection of the surface normal onto a (0001) plane and the nearest <11-20> direction.

SUBSTRATE	EPITAXY
6” N-Type	6” N-Type
8” N-Type	8” N-Type
8” Optical	

### FLATLENGTH

Linear dimension of the flat measured with automated optical micrometer on a sample of one wafer Per boule (see Figure 1).

### PRIMARY FLAT

The flat of the longest length on the wafer, oriented such that the chord is parallel with a specified Low-index crystal plane.

### PRIMARY FLAT ORIENTATION

The primary flat is the (1-100) plane with the flat face parallel to the <11-20> direction. Measured with XRD back reflection technique.

### NOTCH

The notch position is parallel to the <11-20> direction, with the notch bisector is in the (1-100) plane (see Figure 2).

### MARKING\*

For silicon face polished material, the carbon face of each individual wafer is laser-marked with OCR compatible font, similar to definitions and characteristics in SEMI M12. The laser markings are positioned upright when the major flat or notch is oriented up, making the scribe easier to read when the wafers are loaded into cassettes. This format includes a wafer supplier identification code, validating the wafer’s authenticity. It also includes a checksum, which is an error-detection method that prevents OCR mis-read errors and reduces the instance of processing errors associated with such events.

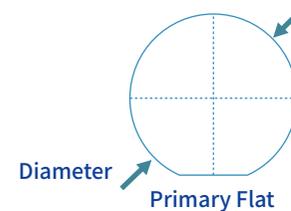


Figure1. Diameter, primary flat location and marking orientation, carbonface up for silicon face polished 150mm n-type wafers

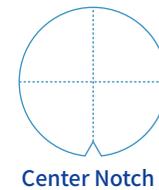


Figure2. Notch location and marking orientation, carbonface up for 200mm 200mm n-type wafers

Note: \* SEMI M12 coding rule is only for 200 mm wafer.

## 6 Inch N-type SiC Substrate

Product Performance	U grade	P grade	D grade
<b>1. Crystal Parameters</b>			
Polytype	4H		
Polytype Areas	None	None	Cumulative area $\leq 10\%$
Micropipe Density	$\leq 0.05$ ea/cm <sup>2</sup>	$\leq 0.1$ ea/cm <sup>2</sup>	$\leq 5$ ea/cm <sup>2</sup>
Resistivity	0.015–0.025 $\Omega \cdot \text{cm}$	0.015–0.025 $\Omega \cdot \text{cm}$	$\leq 0.028 \Omega \cdot \text{cm}$
Basal Plane Dislocation*	$\leq 800$ ea/cm <sup>2</sup>	$\leq 3000$ ea/cm <sup>2</sup>	N/A
Threading Screw Dislocation*	$\leq 100$ ea/cm <sup>2</sup>	$\leq 150$ ea/cm <sup>2</sup>	N/A
Threading Edge Dislocation*	$\leq 2500$ ea/cm <sup>2</sup>	$\leq 5000$ ea/cm <sup>2</sup>	N/A
Surface Metal Contamination	$\leq 5E10$ atoms/cm <sup>2</sup> (Na,K,Ca,Fe,Ni,Cu,Zn,Au,Ag,Al,Ga,Hg,As,Pt)		
<b>2. Mechanical Parameters</b>			
Diameter	150.0 mm $\pm 0.2$ mm		
Wafer Surface Orientation	4° towards <11-20> $\pm 0.2^\circ$	4° towards <11-20> $\pm 0.5^\circ$	
Orthogonal Misorientation	$\pm 5^\circ$	N/A	
Primary Flat Length	47.5 mm $\pm 1.5$ mm	47.5 mm $\pm 2.5$ mm	
Primary Flat orientation	<11-20> $\pm 2^\circ$	<11-20> $\pm 5^\circ$	
Surface finish	Optical polish: Carbon face, CMP: Si face ready for EPI		
Wafer edge	Chamfer		
Roughness (10 $\mu\text{m} \times 10 \mu\text{m}$ )	Si-face: Ra $\leq 0.2$ nm; C-face: Ra $\leq 0.5$ nm		
Thickness	350 $\mu\text{m} \pm 25 \mu\text{m}$		
Total Thickness Variation	$\leq 5 \mu\text{m}$	$\leq 8 \mu\text{m}$	$\leq 10 \mu\text{m}$
Local Thickness Variation (10 mm x 10 mm)	$\leq 2 \mu\text{m}$	$\leq 3.5 \mu\text{m}$	$\leq 3.5 \mu\text{m}$
Bow (Absolute value)**	$\leq 25 \mu\text{m}$	$\leq 25 \mu\text{m}$	$\leq 60 \mu\text{m}$
Warp**	$\leq 40 \mu\text{m}$	$\leq 40 \mu\text{m}$	$\leq 70 \mu\text{m}$
<b>3. Surface Parameters</b>			
Chips/indents	None	$\leq 5$ ea, each depth and width $\leq 1$ mm	
Scratches Si-side	Total Length $\leq 100$ mm		N/A
Total Usable Area (3 mm x 3 mm)	$\geq 95 \%$	$\geq 92 \%$	N/A
Cracks/stains	None		
Edge Exclusion	3 mm		

Note: \* Measured after KOH etching \*\* Measured with FRT

## 8 Inch N-type SiC Substrate

Product Performance	U grade	P grade	D grade
<b>1. Crystal Parameters</b>			
Polytype	4H		
Polytype Areas	None	None	Cumulative area $\leq 10\%$
Micropipe Density	$\leq 0.05$ ea/cm <sup>2</sup>	$\leq 0.1$ ea/cm <sup>2</sup>	$\leq 5$ ea/cm <sup>2</sup>
Resistivity	0.015–0.025 $\Omega \cdot \text{cm}$	0.015–0.025 $\Omega \cdot \text{cm}$	$\leq 0.028 \Omega \cdot \text{cm}$
Basal Plane Dislocation*	$\leq 1000$ ea/cm <sup>2</sup>	$\leq 2000$ ea/cm <sup>2</sup>	N/A
Threading Screw Dislocation*	$\leq 200$ ea/cm <sup>2</sup>	$\leq 300$ ea/cm <sup>2</sup>	N/A
Threading Edge Dislocation*	$\leq 2000$ ea/cm <sup>2</sup>	$\leq 4000$ ea/cm <sup>2</sup>	N/A
Surface Metal Contamination	$\leq 5E10$ Atoms/cm <sup>2</sup> (Na,K,Ca,Fe,Ni,Cu,Zn,Au,Ag,Al,Ga,Hg,As,Pt)		
<b>2. Mechanical Parameters</b>			
Diameter	200.0 mm $\pm 0.2$ mm		
Wafer Surface Orientation	4° towards <11-20> $\pm 0.2^\circ$	4° towards <11-20> $\pm 0.5^\circ$	
Orthogonal Misorientation	$\pm 5^\circ$	N/A	
Notch orientation	<1-100> $\pm 1^\circ$		
Notch Depth	1~1.25 mm		
Surface finish	Optical polish: Carbon face, CMP: Si face ready for EPI		
Wafer edge	Chamfer		
Roughness (10 $\mu\text{m} \times 10 \mu\text{m}$ )	Si-face: Ra $\leq 0.2$ nm; C-face: Ra $\leq 0.5$ nm		
Thickness	350/500 $\mu\text{m} \pm 25 \mu\text{m}$		
Total Thickness Variation	$\leq 5 \mu\text{m}$	$\leq 10 \mu\text{m}$	$\leq 20 \mu\text{m}$
Local Thickness Variation (10 mm x 10 mm)	$\leq 2 \mu\text{m}$	$\leq 5 \mu\text{m}$	$\leq 15 \mu\text{m}$
Bow (Absolute value)	$\leq 15 \mu\text{m}$	$\leq 30 \mu\text{m}$	$\leq 60 \mu\text{m}$
Warp	$\leq 30 \mu\text{m}$	$\leq 60 \mu\text{m}$	$\leq 70 \mu\text{m}$
<b>3. Surface Parameters</b>			
Chips/indents	None	$\leq 5$ ea, each depth and width $\leq 1$ mm	
Scratches Si-side	Total Length $\leq 100$ mm		N/A
Total Usable Area (3 mm x 3 mm)	$\geq 95 \%$	$\geq 92 \%$	N/A
Cracks/stains	None		
Edge Exclusion	3 mm		

Note: \* Measured after KOH etching